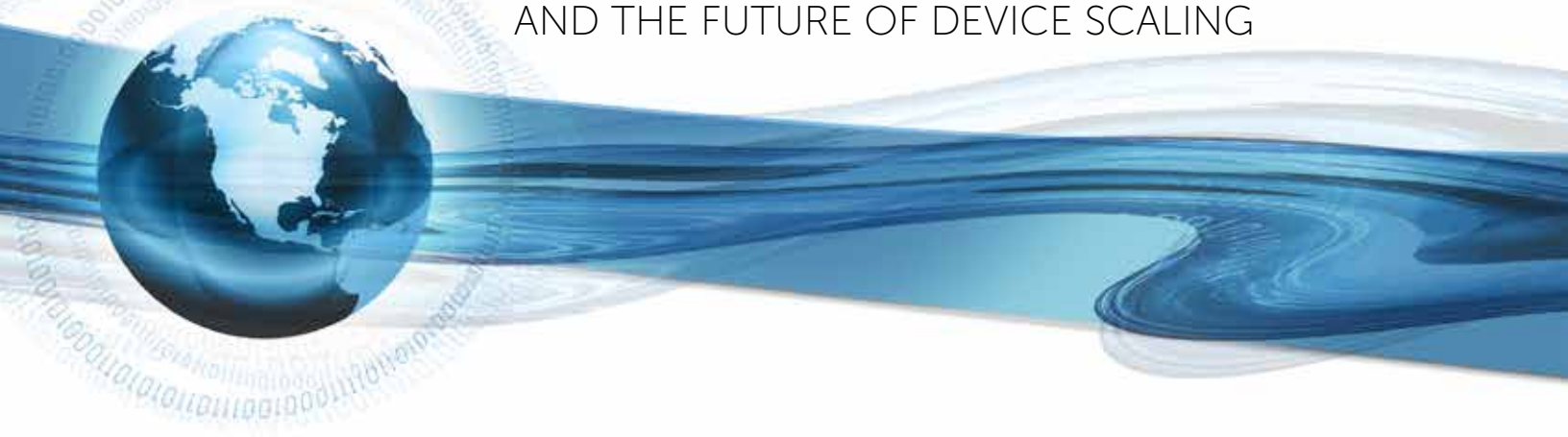
COURSE OFFERING

course title:

14nm FinFET Fabrication

FABRICATION DETAILS, ISSUES & SOLUTIONS
AND THE FUTURE OF DEVICE SCALING



Fabricating 3D FinFET transistors presents a series of novel processing challenges ...

duration:

One Day

course brief:

This advanced course presents a detailed step-by-step description of a 14nm FinFET fabrication process for Bulk silicon and SOI. Gate-last methodologies are presented as well as an introduction to the 10nm FinFET and candidates for sub-10nm devices.

Instructor:

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FinFET Fabrication

DETAILS, ISSUES, AND SOLUTIONS

course objectives:

1) to provide a detailed step-by-step description of the front-end and back-end manufacturing process flow for a 14nm FinFET

2) to present a detailed description of the unique structural characteristics and processing requirements for each fabrication module in a 14nm process flow

3) to introduce the changes that will be present at the 10nm node and to preview future nodes (<10nm)

appropriate for:

Device, test and process engineers, design engineers, equipment and failure anaylisis engineers, managers and other personnel who desire a deeper understanding 14nm FinFet processing.

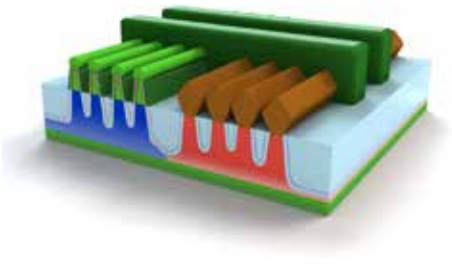
course outline:

14nm FinFET Fabrication:

- Introduction to the basic modules
- Shallow Trench Isolation & Well formation - the new reality
- STI for FinFET-on-bulk versus STI for FinFET-on-SOI
- Fin Fabrication: Self-Aligned Double Patterning (SADP)
- FinFET gate-last Hi-k/Metal Gate integration methodology
- Replacement gate metallurgy & integration strategies for FinFETs
- Strained silicon using SiC and SiGe replacement Source/Drains
- Titanium "Salicidation" integration methodology
- Key FinFET fabrication issues and their solutions
- Line-Etch-Line-Etch (LELE) Double patterning
- SADP for Gate electrode fabrication & the first four layers of metal
- Air gap dielectrics
- Back-end capacitor formation details

The Future:

- How will the 10nm FinFET differ from the 14nm FinFET?
- What options are available for the 10nm node?
- Nanowires - the sub-10nm node option



The course content is presented in a clear, highly visual and easy-to-understand manner. It is taught by a world-class instructor who has over 25 years of hands-on experience in the field of silicon fabrication and who is an award winning public speaker.

The course notes are technically current, reproduced in high resolution color and profusely illustrated with high-quality 3D graphics and TEMs of real-world devices.

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