Course Content:

1. Detailed step-by-step 20 nm front-end planar fabrication process
2. Detailed step-by-step 14 nm FinFET fabrication process (front-end & backend)
3. Detailed 7 nm Vertical Nanowire fabrication sequence
4. FinFET manufacturing issues and solutions
5. 3D Flash fabrication details and manufacturing issues
6. Future memory technologies
7. Advanced Lithography: EUV, DSA, Multi-Patterning
8. 3D Packaging Versus 3D Monolithic status update
9. Extensive SEM/TEM Survey of Leading-edge devices
10. CMOS Technology Forecast: 10 nm, 7 nm, & 5 nm node processing challenges & solutions
This is the one course that you need to attend this year to learn about the key technical breakthroughs in Logic and Memory devices that have enabled 14nm node technology, and the manufacturing challenges of 3D Flash, 10nm FinFETs and 7nm Nanowires.

The central theme of this seminar is an in-depth presentation of the key 20/14/10 nm node technical issues: FinFET implementation, Gate-Last high-k/metal gate implementation, 3D Flash Fabrication, CD control, immersion and EUV lithography, Copper/low-k integration, 3D packaging, Monolithic 3D, and their critical processing issues. Each section of the course will present the relevant technical problems in a clear and comprehensible fashion as well as discuss the proposed range of solutions and equipment requirements necessary to resolve each of these problems.

**seminar contents**

   - The enduring myth of a technology node
   - Market forces: the shift to mobile
   - Ion/Ioff curves, scaling methodology

2. Detailed 20nm Fabrication Sequence. The key to rapidly understanding any new technology is to view it in its entirety.
   - A detailed step-by-step 20nm fabrication process flow
   - High-k/Metal gate and salicide integration techniques
   - Gate-first and Gate-Last integration methodologies
   - Strain Methodologies

3. Detailed 14nm FinFET Fabrication Sequence.
   - A detailed step-by-step 14nm FinFET fabrication process
   - Bulk and SOI FinFET integration
   - FinFET High-k/Metal Gate integration
   - Contact options, including Copper contacts
   - Details of Back-End metallization

4. The transition to 14 nm Node Technology.
   - Self Aligned Double & Quadruple Patterning
   - Increasing FinFET Pitch density
   - NMOS strain fabrication methodology
   - The scalability of three-dimensional device structures
   - 14 nm versus 22 nm; what’s the same, what’s different?

5. The 7nm Node: Nanowires?
   - Horizontal versus vertical Nanowires, what option is optimal for high performance?
   - The advantages of gate-all-around and ALD deposited gate electrodes versus lithographically defined gate electrodes
   - Detailed step-by-step 7nm Nanowire fabrication sequence

6. 3D Flash - Flash Memory Gains New Life
   - A detailed 3D Flash fabrication process will be presented
   - 3D Flash options, manufacturing issues and fabrication strategies
   - Future memory technologies

7. Advanced Lithography. Lithography is the “heartbeat” of semiconductor manufacturing and is also the single most expensive operation in any fabrication process.
   - Double, triple and quadruple patterning techniques
   - Resolution Enhancement Technologies
   - EUV Lithography: status, problems and solutions
   - Emerging Lithography Technologies (DSA, Imprint)

8. Survey of leading edge devices. This part of the course presents a visual feast of TEMs and SEMs of real-world, leading edge devices for Logic, DRAM and Flash memory.

9. 3D Packaging versus Monolithic 3D - which way to go?
   - TSV technology: design, processing and production
   - Interposers: the shortcut to 3D packaging
   - Monolithic 3D fabrication processes
   - Annealing 3D Monolithic structures

    - The two possible paths forward in CMOS Logic device architecture (FinFETs vs UTB FDSOI)
    - The transition to 3D devices (Logic & 3D Flash Memory)
    - Future memory technologies: OVM, RRAM, PCRAM and Crossbar Memory
    - New nanoscale effects and their impact on CMOS device architecture and materials
    - Future devices: Quantum well devices and Tunnel FETs
    - Is Moore’s law finally coming to an end?
what's included

1) Three days of instruction by industry experts with in-depth knowledge of the subject material.
2) A superlative set of full-color notes including SEM & TEM micrographs of real-world device structures that illustrate key technical features and manufacturing challenges.
3) Continental breakfast, hot buffet lunch & morning and afternoon refreshments served daily.

who should attend

• Equipment Suppliers & Metrology Engineers
• Fabless Design Engineers and Managers
• Foundry Interface Engineers and Managers
• Device and Process Engineers
• Design Engineers

Tuition $1,695

• Product Engineers
• Process Development & Process Integration Engineers
• Process Equipment Marketing Managers
• Materials Supplier Marketing Managers & Applications Engineers

course instructors

The best instructors in the business will be teaching this course. All of the instructors are world-class experts in their respective fields, with decades of industry experience. However, these presenters have been selected not just for their deep technical expertise, but also for their ability to present complex technical information in a clear and engaging manner. Each of these instructors is an experienced and skilled public speaker, and the accompanying course notes for this seminar are profusely illustrated with high-quality 3D color graphics and relevant SEMs and TEMs. We want you to leave this course with a clear understanding of the key enabling technologies that have made the 14nm node technology a reality, as well as an understanding what the central technical challenges are for the 10/7 nm nodes. After you have completed this course you will never again leave a meeting wondering what people were talking about.

Jerry Healey has been a technical professional in the semiconductor industry for over 25 years, 8 years of which were spent as a Device Engineer at Motorola Semiconductor. He was formerly an instructor for UC Berkeley Extension (College of Engineering), and was also employed as a Process Integration Engineer at both Sematech and the Advanced Technology Development Facility, where he worked on advanced technology node development.

He is a renowned lecturer in the field of silicon processing, and his areas of expertise include process integration, technology transfer of new processes from R&D into manufacturing, 3D Packaging versus 3D Monolithic Packaging, and FinFET fabrication. His audiences remember him for the breadth of his knowledge regarding semiconductor manufacturing, his engaging lecture style, and the insightful color graphics he uses to illustrate his lectures.

Dr. Moshe Preil is the Manager of Emerging Lithography Technology at Global Foundries. He directs a team that is tasked with investigating state-of-the-art Lithography tools and processes such as Directed Self Assembly (DSA), e-Beam Direct Write (EBDW) and EUV lithography. His current work also includes developing methods to control overlay and critical dimensions to improve advanced lithography processes and enable the extension of lithography to the 10nm node and beyond.

Dr. Preil has 25 years of experience in the field of advanced lithography working for ASML, KLA-Tencor, and Advanced Micro Devices. A dramatic and engaging public speaker, Dr. Preil has taught numerous courses on the subject of optical lithography, has published extensively in this field, and is widely regarded as a gifted and inspiring instructor.

Dick James is the Senior Technology Analyst for Chipworks, an Ottawa, Canada-based reverse engineering company that specializes in semiconductors and electronic systems.

Dick joined Chipworks in 1995 and acts as a consultant to Chipworks’ staff and customers, dealing with the micro-structural characterization of devices, both process and packaging. He is also a much sought-after speaker at technical conferences and a popular blogger at Chipworks.com and ElectroIQ.com, and occasionally writes articles for other publications.

Dick graduated in 1971 with a M.Sc. in Microelectronics and Semiconductor Devices from the University of Southampton in England, and a B.Sc. in Applied Chemistry from the University of Salford. He has over 40 years’ experience in process development, design, manufacturing, packaging and reverse engineering of semiconductor devices.