1. Detailed step-by-step 14/10 nm FinFET fabrication process (front-end & back-end)
2. FinFET manufacturing issues and solutions
3. 7/5 nm Nanowire fabrication
4. Planar Flash & DRAM Memory Fabrication
5. Detailed 3D Flash fabrication process flow and discussion of manufacturing issues
6. Future memory technologies
7. Extensive SEM/TEM Survey of Leading-edge devices
8. 3D Packaging Versus 3D Monolithic packaging status update
9. CMOS Technology Forecast: 5 nm, 3.5 nm, 2.5 nm nodes
Advanced CMOS Technology
THE 14/10/7 NM NODES

This is the one course that you need to attend this year to learn about the key technical breakthroughs in Logic and Memory that have enabled 14/10nm node technology, and the manufacturing challenges of 3D Flash, 7nm FinFETs and 5nm Nanowires.

introduction

The central theme of this seminar is an in-depth presentation of the key 14/10/7nm node technical issues: FinFET fabrication, Gate-Last high-k/metal gate implementation, 3D Flash Fabrication, CD control, immersion and EUV lithography, Copper/low-k integration, 3D packaging, Monolithic 3D, and their critical processing issues. Each section of the course will present the relevant technical problems in a clear and comprehensible fashion as well as discuss the proposed range of solutions and equipment requirements necessary to resolve each of these problems.

seminar contents

   - The enduring myth of a technology node
   - Market forces: the shift to mobile
   - The Idsat equation
   - Ion/Ioff curves, scaling methodology

2. Detailed 14/10nm FinFET Fabrication Sequence. The FinFet represents a radical departure in transistor architecture.
   - A detailed step-by-step 14/10 nm FinFET fabrication process
   - Bulk and SOI FinFET integration
   - FinFET High-k/Metal Gate integration
   - Contact options, including Cobalt contacts
   - Details of Back-End metallization methodologies and air-gap dielectrics

3. The 7/5 nm Node; Nanowires?
   - A Vertical Nanowire fabrication process
   - Key fabrication details and manufacturing problems
   - Vertical versus horizontal Nanowires: advantages and disadvantages
   - Nanowire SCE control and scaling

4. Planar Flash & DRAM Memory.
   - DRAM memory function and nomenclature
   - DRAM scaling limits
   - The capacitor-less DRAM memory cell
   - Planar Flash operation and function
   - Planar Flash scaling techniques

5. 3D Flash Memory
   - A detailed step-by-step Samsung 3D NAND Flash fabrication process
   - Staircase fabrication methodology
   - The role of ALD in 3D Flash fabrication
   - The Intel-Micron 3D NAND process
   - The Toshiba BICS 3D NAND process

6. Advanced Lithography.
   - Physical Limits of Lithography Tools
   - Immersion Lithography – principles and practice
   - Double, Triple and Quadruple patterning
   - EUV Lithography: status, problems and solutions
   - Resolution Enhancement Technologies
   - Photoresist: chemically amplified resist issues
   - Emerging Lithography Technologies (DSA, Imprint etc.)

7. Emerging Memory Technologies.
   - Detailed Cross-point memory process flow
   - Phase Change Memory (PCRAM)
   - Resistive RAM (ReRAM) – novel and comes in two variations
   - Spin Torque Transfer RAM (STT-RAM) – the brightest prospect?

8. Survey of leading edge devices. This part of the course presents a visual feast of TEMs and SEMs of real-world, leading edge devices for Logic, DRAM and Flash memory.

9. 3D Packaging versus Monolithic 3D - which way to go?
   - TSV technology: design, processing and production
   - Interposers: the shortcut to 3D packaging
   - Monolithic 3D fabrication processes
   - Annealing 3D Monolithic structures
   - The Internet of Things (IoT).

    - The two possible paths forward in CMOS Logic device architecture (FinFETs vs. UTB FDSOI)
    - The transition to 3D devices (Logic & Flash Memory)
    - New nanoscale effects and their impact on CMOS device architecture and materials
    - Future devices: Quantum well devices, Tunnel FETs and Quantum Wires
    - Is Moore’s law finally coming to an end?
**what’s included**

1) Three days of instruction by industry experts with in-depth knowledge of the subject material.

2) A superlative set of full-color notes including SEM & TEM micrographs of real-world device structures that illustrate key technical features and manufacturing challenges.

3) Continental breakfast, hot buffet lunch and morning and afternoon refreshments served daily.

**who should attend**

- Equipment Suppliers & Metrology Engineers
- Fabless Design Engineers and Managers
- Foundry Interface Engineers and Managers
- Device and Process Engineers
- Design Engineers

**course instructors**

The best instructors in the business will be teaching this course. All of the instructors are world-class experts in their fields, with decades of industry experience. However, these presenters have been selected not just for their deep technical expertise, but also for their ability to present complex technical information in a clear and engaging manner. Each of these instructors is an experienced and skilled public speaker, and the accompanying course notes for this seminar are profusely illustrated with high-quality 3D color graphics and relevant SEMs and TEMs. We want you to leave this course with a clear understanding of the key enabling technologies that have made the 14/10/7nm node technologies a reality, as well as an understanding of what the central technical challenges are for the 10/7 nm nodes. After you have completed this course you will never again leave a meeting wondering what people were talking about.

**Jerry Healey** has been a technical professional in the semiconductor industry for over 25 years, 8 years of which were spent as a Device Engineer at Motorola Semiconductor. He was formerly an instructor for UC Berkeley Extension (College of Engineering), and was also employed as a Process Integration Engineer at both Sematech and the Advanced Technology Development Facility, where he worked on advanced technology node development. He is a renowned lecturer in the field of silicon processing, and his areas of expertise include process integration, technology transfer of new processes from R&D into manufacturing, 3D Packaging versus 3D Monolithic Packaging, and FinFET fabrication. His audiences remember him for the breadth of his knowledge regarding semiconductor manufacturing, his engaging lecture style, and the insightful color graphics he uses to illustrate his lectures.

**Dr. Moshe Preil** is a world-class lithographer with over 30 years of experience in the field. He has worked at AMD, Luminescent, ASML and most recently he was the Manager of Emerging Lithography Technology at Global Foundries. Currently he is the Senior Marketing Manager in the Patterning Division at KLA-Tencor. He has lead teams tasked with investigating state-of-the-art Lithography tools and processes such as Directed Self Assembly (DSA), e-Beam Direct Write (EBDW) and managed an EUV lithography tool. A dramatic and engaging public speaker, Dr. Preil has taught numerous courses on the subject of optical lithography, has published extensively in this field, and is widely regarded as a gifted and inspiring instructor.

**Dick James** is the Technology Analyst Emeritus for TechInsights, an Ottawa, Canada-based reverse engineering company that specializes in semiconductors and electronic systems.

Dick joined TechInsights predecessor, Chipworks, in 1995 and acts as a consultant to TechInsights’ staff and customers, dealing with the microstructural characterization of devices, both process and packaging. He is also a much sought-after speaker at technical conferences and a popular blogger at TechInsights.com and ElectroIQ.com, and other publications.

Dick graduated in 1971 with a M.Sc. in Microelectronics and Semiconductor Devices from the University of Southampton in England, and a B.Sc. in Applied Chemistry from the University of Salford. He has over 40 years’ experience in process development, design, manufacturing, packaging and reverse engineering of semiconductor devices.

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**Tuition** $1,795

**who should attend**

- Product Engineers
- Process Development & Process Integration Engineers
- Process Equipment & Marketing Managers
- Materials Supplier Marketing Managers & Applications Engineers

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