Jerry T. Healey

(512) 576-6404
4949 Hamilton Wolfe Road, Suite 6103
San Antonio Texas, 78229
jhealey@thresholdsystems.com

Professional Experience:

President - Threshold Systems (www.thresholdsystems.com) 1998 - 2004
P.O. Box 321, Springdale, Utah, 84767 2006 - present

- Manage a consulting firm which specializes in:
  - short course technology instruction for senior scientists and engineers in the subjects of Process Integration, Advanced CMOS Manufacturing, and 3D packaging
  - technical consulting for client companies regarding Technology Road Maps, identifying research and development opportunities, and preparing research reports on emerging technologies
  - provide advice and resolution strategies to manufacturer's on process integration issues and yield optimization
  - expert witness for litigation involving semiconductor processing and IP issues
  - qualification of semiconductor fabrication facilities for clients and yield crisis resolution

Expert Witness *April 2008 -* Oct. 2009

- Acted as the lead expert witness in a multibillion dollar litigation between two major Chinese semiconductor companies (TSMC vs. SMIC)
- Conducted a detailed analysis of four generations of microchip process flows to ascertain the veracity of trade secret claims
- Examined in excess of 1,000 papers and patents in a prior art search to establish that certain trade secret claims were publicly available and/or readily ascertainable
- Testified in an eight-hour deposition as well as took the stand for three hours in Federal court in Alameda County California, to opine on the validity of specific trade secret claims

Baseline Integration Engineer
Sematech's Advanced Technology Development Center (ATDF) April 2004 – Jan. 2006

- Managed an 90nm research baseline and was responsible for leading teams of engineers to resolve all technical issues associated with this process flow and for maintaining the line stability
- Resolved processing issues on a leading-edge high-k/metal gate logic process flow
- Acted as the key development engineer on the ATDF 45nm development effort, assuming responsibility for engineering the transistor gate stack
- Interfaced with Front End Process R&D on a daily basis and addressed their fabrication concerns, as well as integrated their new process modules into the baseline process

Instructor - UC Berkeley Extension, College of Engineering 1995 - 2004
University of California at Berkeley, Berkeley, California

- A key lecturer for UC Berkeley's public courses on the subjects of Process Integration for the highly acclaimed courses: "Silicon processing for the VLSI Era", "Process Integration for Sub-Micron Technologies"

Senior Process Integration Engineer
Motorola Semiconductor Products Sector, **MOS 8**, Austin, Texas. 1994 - 1998

- Orchestrated the transfer of a range of high performance Logic parts featuring embedded Non-Volatile memory elements from Motorola's research facility (APRDL) into a manufacturing environment, and solved numerous process integration problems associated with these devices
- Made numerous presentations to senior management and Design and Process Engineering staffs, as well as directly to customers

Technology Transfer Device Engineer **- Advanced Microcontrollers**

Motorola Semiconductor Products Sector, **MOS 8**, Austin, Texas. 1993 - 1994

- Successfully transferred numerous 16/32-bit microcontrollers and other complex multi-function Logic devices from R&D into high-volume production, and systematically enhanced their yields
- Interfaced with Design, Test, Product Engineering, and Manufacturing, and lead cross-functional groups to resolve technical problems associated with the manufacture of state-of-the-art ICs

Device Engineer

MOS 8 Motorola Semiconductor Products Sector, Austin, Texas. 1991 - 1993

- Managed the production of a large portfolio of digital/analog Logic devices for Custom Automotive, Telecom, and Advanced Microcontroller Systems
- Designed experiments to isolate and identify the sources of yield loss and conducted failure analysis to successively enhance the yield of these devices

Education:

Master of Science - Semiconductor Physics Graduated 1991
University of Utah, Salt Lake City, Utah.

Bachelor of Science - Science Graduated 1984
University of Waterloo, Waterloo Ontario, Canada.

Special Skills:

- Excellent communication skills - written and verbal
- Outstanding people skills

Activities:

- Technical rock climbing, technical ice climbing, rowing, bicycling, canyoneering

Publications:

Papers

- Jerry Healey & Craig Franklin**, "The Prevention of Polyimide Stringers on Bonding Pads",** *Interface '93 Microlithography Seminar Proceedings*; September 1993.

- Jerry Healey & George Kong**,"The Reduction of Low-Level Current Leakage in CMOS Devices"**, *Microelectronics Manufacturability, Yield, and Reliability*, October 1994.

- Jerry Healey, Tony Phan & Randy Kent**,"The Prevention of Auto Doping induced Threshold Voltage Shifts"**, *SPIE The International Society for optical Engineering*, October 1, 1995.

- Jerry Healey & Tony Phan **,"The Role of RIE in Microchip Bond Pad Corrosion";** *SPIE The International Society for optical Engineering*, October 16, 1996.

- Jerry Healey & Neil Henis**,"Yield Enhancement Through Monitoring of Real Time Manufacturing Processes"**, *Future Fab International*, January 1, 1997.

- Jerry Healey & Scott Rubel **,"The Influence of Topographical Variations on Reliable Via and Contact Formation",** *Microelectronics Manufacturability, Yield, and Reliability*, August 1999.

- Jerry Healey, "**Dual Damascene and Low-K Dielectrics",** web publication, www.siliconnexus.com, 2002. (17,000 copies downloaded).

- Jerry Healey, Dave Dyer, Chuck Stager**,** Diane Michaleson**, "The Prevention of Cobalt Silicide Stringers on Nitride Spacers",** web publication, www.siliconnexus.com, 2006. (9,500 copies downloaded).

Publications CD ROMs:

- Jerry Healey **"Chemical Mechanical Polishing",** an instructional CD ROM and accompanying course text; *Threshold Systems*, August 2001.

Patents:

- Jerry Healey, David Brady**,** Todd Rhoad **"A Method for Controlling the Etch Rate of Silicon Dioxide Offset Spacers"**; ATDF Application.