ADVANCED CMOS TECHNOLOGY 2019

(The 10/7/5 nm Nodes)

May 15, 16, 17, 2019, Milpitas California

COURSE CONTENT IS UPDATED & TECHNICALLY CURRENT THROUGH MAY 2019

INCLUDES: 10/7 NM FINFET, 3D FLASH AND NANOWIRE FABRICATION DETAILS

1. Detailed step-by-step 10 nm FinFET fabrication process (front-end & back-end)
2. FinFET manufacturing issues and solutions
3. 5 nm Horizontal Nanowire fabrication process flow
4. DRAM Memory Fabrication and Yield Issues
5. Detailed 3D Flash fabrication process flow and manufacturing issues
6. Future memory technologies
7. Extensive SEM/TEM Survey of Leading-edge devices
8. EUV Applications, Power Solutions and Status Update
9. 3D Packaging Versus 3D Monolithic packaging status update
10. CMOS Technology Forecast: 5 nm, 3.5 nm, 2.5 nm nodes

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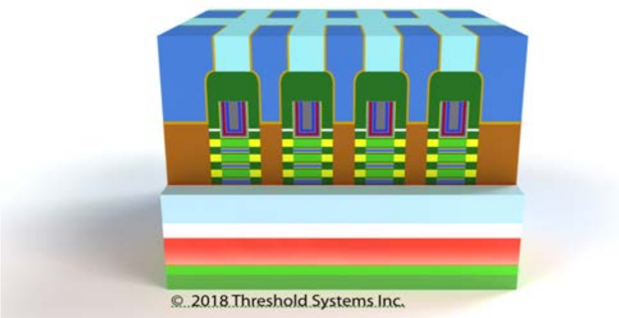
Advanced CMOS Technology

THE 10/7/5 NM NODES



This is the best and the most important course that you can attend this year to learn about the key technical break-throughs in Logic and Memory that have enabled 10/7 nm node technology, and the manufacturing challenges of 3D Flash, 7 nm FinFETs and 5 nm Nanowires.

introduction

The central theme of this seminar is an in-depth presentation of the key 10/7/5 nm node technical issues: FinFET fabrication, Nanowire fabrication, DRAM & 3D Flash Fabrication, CD control, immersion and EUV lithography, Copper/low-k integration, 3D packaging, Mono-lithic 3D, and their critical processing issues. Each section of the course will present the relevant technical problems in a clear and com-prehensible fashion as well as discuss the proposed range of solutions and equipment requirements necessary to resolve each of these problems. High quality 3D graphics are used throughout the course as well as SEMs and TEMs of the latest microelectronic devices.

seminar contents

1. Process integration. The 10/7 nm technology nodes represent landmarks in semiconductor manufacturing.
   - The enduring myth of a technology node
   - Market forces: the shift to mobile applications
   - The Idsat equation
   - Ion/Ioff curves, scaling methodology

2. Detailed 10/7 nm FinFET Fabrication Sequence. The FinFet represents a radical departure in transistor architecture.
   - A detailed step-by-step 10/7 nm FinFET fabrication process
   - FinFET High-k/Metal Gate integration
   - Cobalt contacts and Cobalt metal lines
   - Details of Back-End metallization methodologies and air-gap dielectrics

3. Nanowires at the 5 nm Node
   - The drive to Gate-All-Around (GAA) devices
   - Nanowire SCE control and scaling
   - A detailed 5nm Nanowire fabrication process
   - Key fabrication details and manufacturing problems
   - Vertical versus horizontal Nanowires: advantages and disadvantages

4. Planar Flash & DRAM Memory.
   - DRAM memory function and nomenclature
   - DRAM scaling limits
   - The capacitor-less DRAM memory cell
   - Planar Flash operation and function
   - Planar Flash scaling techniques

5. 3D Flash Memory
   - A detailed step-by-step Samsung 3D NAND Flash fabrication process
   - Staircase fabrication methodology
   - The role of ALD in 3D Flash fabrication
   - The Intel-Micron 3D NAND process
   - The Toshiba BICS 3D NAND process

6. Advanced Lithography.
   - Physical Limits of Lithography Tools
   - Immersion Lithography – principles and practice
   - Double, Triple and Quadruple patterning
   - EUV Lithography: status, problems and solutions
   - Resolution Enhancement Technologies
   - Photoresist: chemically amplified resist issues
   - Emerging Lithography Technologies (DSA)

7. Emerging Memory Technologies.
   - Detailed Cross-point memory process flow
   - Phase Change Memory (PCRAM)
   - Resistive RAM (ReRAM) – novel and comes in two variations
   - Spin Torque Transfer RAM (STT-RAM) – the brightest prospect?

8. Survey of leading edge devices. This part of the course presents a visual feast of TEMs and SEMs of real-world, leading edge devices for Logic, DRAM, and Flash memory. It is presented by Dick James, the Fellow Emeritus of TechInsights.

9. 3D Packaging versus Monolithic 3D - which way to go?
   - TSV technology: design, processing and production
   - Interposers: the shortcut to 3D packaging
   - Monolithic 3D fabrication processes
   - Annealing 3D Monolithic structures
   - The Internet of Things (IoT).

10. The Way forward: a CMOS technology forecast.
    - The transition to 3D devices (Logic & Flash Memory)
    - The Future of Mamory and Logic
    - New nanoscale effects and their impact on future CMOS device architecture and materials
    - Future devices: Quantum well devices, Tunnel FETs and Quantum Wires
    - Is Moore's law finally coming to an end?

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what's included

1) Three days of instruction by industry experts with in-depth knowledge of the subject material.
2) A superlative set of full-color notes featuring hundreds of superb 3D graphics and SEM & TEM micrographs of real-world device structures that illustrate key technical features of these devices.
3) Continental breakfast, hot buffet lunch and morning and afternoon refreshments served daily.

who should attend

- Equipment Suppliers & Metrology Engineers
- Fabless Design Engineers and Managers
- Foundry Interface Engineers and Managers
- Device and Process Engineers
- Design Engineers
- Product Engineers
- Process Development & Process Integration Engineers
- Process Equipment & Marketing Managers
- Materials Suppliers & Applications Engineers
- Patent Attorneys

Tuition $1,795

course instructors

The best instructors in the business teach this course. All of the instructors are world-class experts in their fields, with decades of industry experience. However, these presenters have been selected not just for their deep technical expertise, but also for their ability to present complex technical information in a clear and engaging manner. Each of these instructors is an experienced and skilled public speaker, and the accompanying course notes for this seminar are profusely illustrated with high-quality 3D color graphics and relevant SEMs and TEMs. We want you to leave this course with a clear understanding of the key enabling technologies that have made the 10/7 nm node technologies a reality, as well as an understanding of what the central technical challenges are for the 5 nm node. After you have completed this course you will never again leave a meeting wondering what people were talking about.

Jerry Healey has been a technical professional in the semiconductor industry for 30 years, 8 years of which were spent as a Device Engineer at Motorola Semiconductor. He was formerly an instructor for UC Berkeley Extension (College of Engineering), and was also employed as a Process Integration Engineer at both Sematech and the Advanced Technology Development Facility (ATDF), where he worked on advanced technology node development.

He is a renowned lecturer in the field of silicon processing, and his areas of expertise include process integration, technology transfer of new processes from R&D into manufacturing, Nanowire and FinFET fabrication. His audiences remember him for the breadth of his knowledge regarding semiconductor manufacturing, his engaging lecture style, and the insightful color graphics he uses to illustrate his lectures.

Dr. Moshe Preil is a world-class lithographer with over 30 years of experience in the field. He has worked at AMD, Luminescent, ASML and most recently he was the Manager of Emerging Lithography Technology at Global Foundries. Currently he is the Senior Marketing Manager in the Patterning Division at KLA-Tencor. He has lead teams tasked with investigating state-of-the-art Lithography tools and processes such as Directed Self Assembly (DSA) and e-Beam Direct Write (EBDW) as well as managed an EUV lithography tool. A dramatic and engaging public speaker, Dr. Preil has taught numerous courses on the subject of optical lithography, has published extensively in this field, and is widely regarded as a gifted and inspiring instructor.

Dick James is the Fellow Emeritus for TechInsights, an Ottawa, Canada-based reverse engineering company that specializes in semiconductors and electronic systems.

Dick joined TechInsights predicessor, Chipworks, in 1995 and acts as a consultant to TechInsights' staff and customers, dealing with the microstructural characterization of devices, both process and packaging. He is also a much sought-after speaker at technical conferences and a popular blogger at TechInsights.com and ElectroIQ.com, and other publications.

Dick graduated in 1971 with a M.Sc. in Microelectronics and Semiconductor Devices from the University of Southampton in England, and a B.Sc. in Applied Chemistry from the University of Salford. He has over 40 years' experience in process development, design, manufacturing, packaging and reverse engineering of semiconductor devices and is a world authority on the interpretation and analysis of Scanning and Transmissin Electron Micrographs.