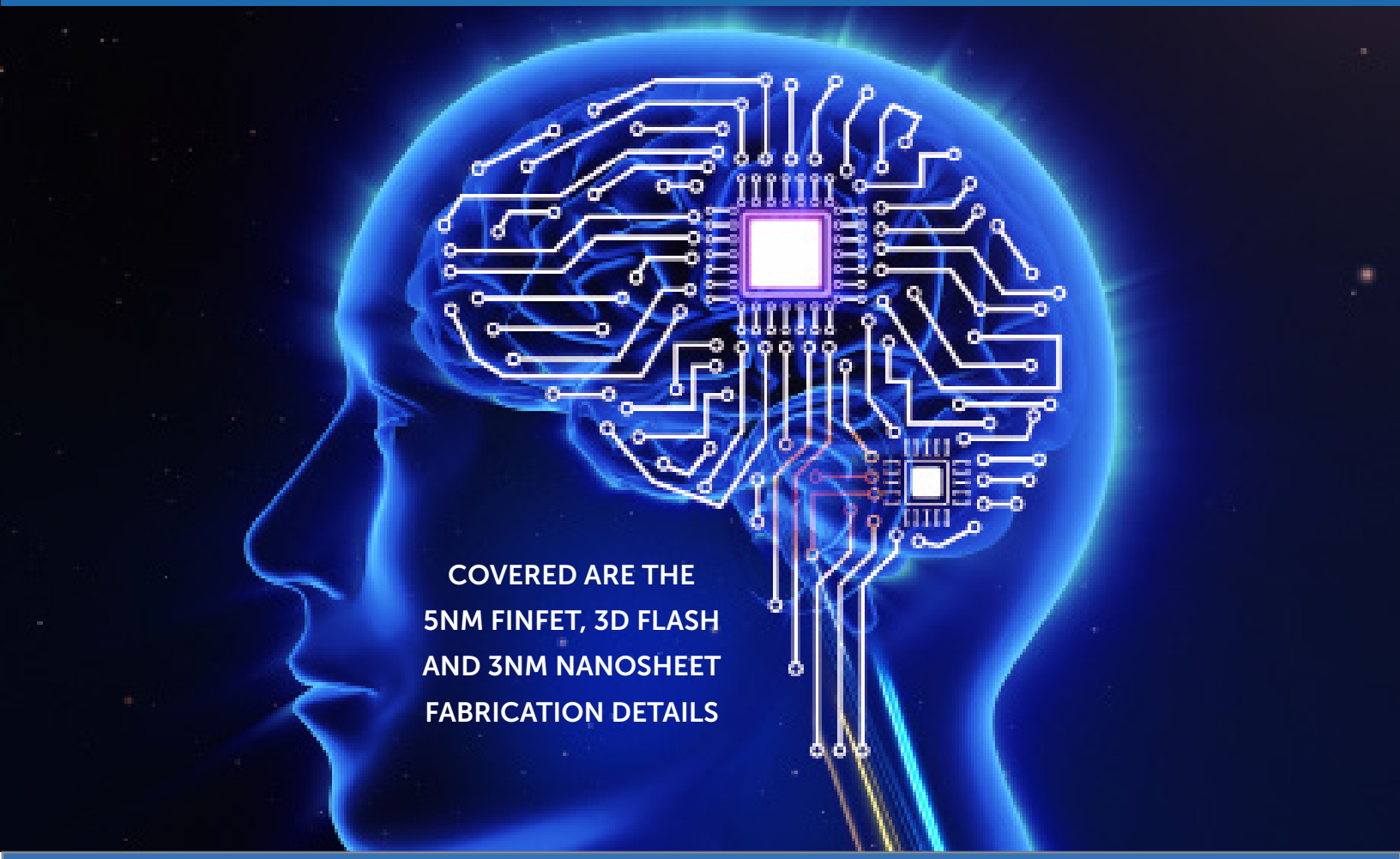
ADVANCED CMOS TECHNOLOGY 2021

An ONLINE Course (The 5/3/2nm Nodes)

COURSE CONTENT IS UPDATED & TECHNICALLY CURRENT AS OF OCTOBER 2021



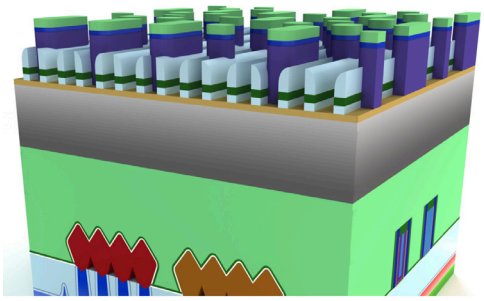
1. Detailed step-by-step 5 nm FinFET fabrication process (front-end & back-end)
2. FinFET manufacturing issues and solutions
3. Step-by-step 3nm Nanosheet fabrication process flow
4. DRAM Memory Fabrication and Yield Issues
5. Detailed 3D Flash fabrication process flow and manufacturing issues
6. Future memory technologies
7. Extensive SEM/TEM Survey of Leading-edge devices
8. EUV Applications, Power Solutions and Status Update
9. 3D Packaging Versus 3D Monolithic packaging status update
10. CMOS Technology Forecast: 2 nm, 1 nm node fabrication innovations

ThresholdSystems

www.ThresholdSystems.com

Advanced CMOS Technology - An Online Course

THE 5/3/2NM NODES



This is the best and the most important course that you can attend this year to learn about the key technical break-throughs in Logic and Memory that have enabled 5 nm node technology, and the manufacturing challenges of 3D Flash, 5nm FinFETs and 3 nm Nanosheets.

Online Learning

The Covid-19 pandemic and the travel restrictions it has imposed have changed the landscape of technical instruction from traditional instructor-lead classroom learning toward a distributed learning experience that enables the instructor and the students to be in socially distant locations. This learning solution eliminates high cost and inconvenience associated with having students travel to one location for instruction. It offers a safe, flexibile, convenient and less expensive learning experience that traditional classroom instruction does not have. It is also ideal for companies with a global business model and whose employees are scattered around the world.

Course Contents

1. Process integration. The 5nm technology nodes represent landmarks in semiconductor manufacturing.
   - The enduring myth of a technology node
   - Market forces: the shift to mobile applications
   - The Idsat equation
   - Ion/Ioff curves, scaling methodology
   - The Standard Cell concept
   - Buried Power Rails

2. Detailed 5nm FinFET Fabrication Sequence. The FinFet represents a radical departure in transistor architecture.
   - A detailed step-by-step 7/5 nm FinFET fabrication process
   - FinFET High-k/Metal Gate integration
   - Cobalt contacts and Cobalt metal lines
   - Contact Over Active Gate
   - Multiple Vt Implementation
   - Tone reversal metallization methodology and air-gap dielectrics
   - Germanium PMOS Fin fabrication

3. Nanosheets at the 3nm Node
   - The drive to Gate-All-Around (GAA) devices
   - Nanosheet SCE control and scaling
   - A detailed 3nm Nanosheet fabrication process
   - Key fabrication details and manufacturing problems

4. Planar Flash & DRAM Memory.
   - DRAM memory function and nomenclature
   - DRAM scaling limits
   - Planar Flash operation and function
   - Planar Flash scaling techniques

5. 3D Flash Memory
   - A detailed step-by-step Samsung 3D NAND Flash fabrication process
   - Staircase fabrication methodology
   - The evolution of 3D NAND Flash
   - Future 3D FLASH implementations

6. Advanced Lithography.
   - Physical Limits of Lithography Tools
   - Immersion Lithography – principles and practice
   - Double and Quadruple patterning
   - EUV Lithography: status, problems and solutions
   - EUV in high-volume manufacturing
   - High Numberical Apeture EUV

7. Emerging Memory Technologies.
   - Phase Change Memory (PCRAM)
   - Resistive RAM (ReRAM)
   - Spin Torque Transfer RAM (STT-RAM) – the brightest prospect?

8. A survey of Leading Edge devices.
   This part of the course presents a visual feast of TEMs and SEMs of real-world, leading edge devices for Logic, DRAM, and Flash memory. It is presented by Dick James, the Fellow Emeritus of TechInsights.

9. 3D Packaging versus Monolithic 3D - which way to go?
   - TSV technology: design, processing and production
   - Interposers: the shortcut to 3D packaging
   - Monolithic 3D fabrication processes
   - Annealing 3D Monolithic structures
   - The Internet of Things (IoT).

10. The Way forward: a CMOS technology forecast.
    - The future of metallization; new approaches and new materials for the 3nm and 2nm nodes
    - The Future of Mamory and Logic
    - New nanoscale effects and their impact on future CMOS device architecture and materials
    - Is Moore's law finally coming to an end?

ThresholdSystems

A 3-DAY ONLINE COURSE

COURSE DATES: OCTOBER 6, 7, 8, 2021

How Online Learning Works:

Shortly after registeration you will be emailed a link that will take you to the online classroom on the day of the course. The week before the class begins a binder of color course notes will be shipped to you via Fedex or UPS.

The class is three days long. On the day of the class you simply click on the link that has been provided and you will be seamlessly taken to the online classroom where you will be able to see, hear and interact with the instructor.

Who Should Attend:

- Equipment Suppliers & Metrology Engineers
- Fabless Design Engineers and Managers
- Foundry Interface Engineers and Managers
- Device and Process Engineers
- Design Engineers
- Product Engineers
- Process Development & Process Integration Engineers
- Process Equipment & Marketing Managers
- Materials Suppliers & Applications Engineers
- Patent Attorneys

Tuition: $1,895

Course Instructors:

The best instructors in the business teach this course. All of the instructors are world-class experts in their fields, with decades of industry experience. However, these presenters have been selected not just for their deep technical expertise, but also for their ability to present complex technical information in a clear and engaging manner. Each of these instructors is an experienced and skilled public speaker, and the accompanying course notes for this seminar are profusely illustrated with high-quality 3D color graphics and relevant SEMs and TEMs. We want you to leave this course with a clear understanding of the key enabling technologies that have made the 5nm node technologies a reality, as well as an understanding of what the central technical challenges are for the 5 nm node. After you have completed this course you will never again leave a meeting wondering what people were talking about.

Jerry Healey has been a technical professional in the semiconductor industry for 30 years, 8 years of which were spent as a Device Engineer at Motorola Semiconductor. He was formerly an instructor for UC Berkeley Extension (College of Engineering), and was also employed as a Process Integration Engineer at both Sematech and the Advanced Technology Development Facility (ATDF), where he worked on advanced technology node development.

He is a renowned lecturer in the field of silicon processing, and his areas of expertise include process integration, technology transfer of new processes from R&D into manufacturing, and Nanosheet and FinFET fabrication. His audiences remember him for the breadth of his knowledge regarding semiconductor manufacturing, his engaging lecture style, and the insightful color graphics he uses to illustrate his lectures.

Dr. Moshe Preil is a world-class lithographer with over 30 years of experience in the field. He has worked at AMD, Luminescent, ASML and was the Manager of Emerging Lithography Technologies at Global Foundries. Currently he is the Senior Technical Manager, Product Strategy at Carl Zeiss SMT. He has lead teams tasked with investigating state-of-the-art Lithography tools and processes such as Directed Self Assembly (DSA) and e-Beam Direct Write (EBDW) as well as managed an EUV lithography tool. A dramatic and engaging public speaker, Dr. Preil has taught numerous courses on the subject of optical lithography, has published extensively in this field, and is widely regarded as a gifted and inspiring instructor.

Dick James is the Fellow Emeritus for TechInsights, a Canadian reverse engineering company that specializes in deprocessing semiconductors and electronic systems.

Dick joined TechInsights predecessor, Chipworks, in 1995 and acts as a consultant to TechInsights' staff and customers, dealing with the microstructural characterization of devices, both process and packaging. He has over 40 years' experience in process development, design, manufacturing, packaging and reverse engineering of semiconductor devices and is a world authority on the interpretation and analysis of Scanning and Transmissin Electron Micrographs.

He is also a much sought-after speaker at technical conferences and a popular blogger at TechInsights.com, Semiconductor Digest and numerous other publications.